Claims

What is claimed is:

1. A semiconductor device comprising:

a transmitter, receiver, and transmission line formed within the semiconductor device, wherein the transmitter, receiver, and transmission line are adapted to control data transfer between a first core and a second core within the semiconductor device, wherein the transmitter is adapted to send a signal over the transmission line to the receiver adapted to receive the signal, wherein the receiver is further adapted to create an impedance mismatch to indicate that the second core is unable to transfer the data, and wherein the transmitter is adapted to detect the impedance mismatch.

2. The semiconductor device of claim 1, wherein the receiver is further adapted to change an impedance of the transmission line to create the impedance mismatch.

3. The semiconductor device of claim 2, wherein the receiver comprises a capacitor adapted to change the impedance of the transmission line.

4. The semiconductor device of claim 1, wherein the transmitter is further adapted to terminate the data transfer upon detection of the impedance mismatch.

5. The semiconductor device of claim 1, wherein the first core and the second core are each selected from the group consisting of a microcontroller, a microprocessor, and an integrated circuit.

6. The semiconductor device of claim 1, wherein the signal is a voltage signal, and wherein the transmitter is adapted to receive a reflection of the voltage signal.

7. The semiconductor device of claim 1, wherein the transmitter comprises a voltage comparator adapted to compare an amplitude of the voltage signal to an amplitude of the reflection of the voltage signal.

8. The semiconductor device of claim 7, wherein the voltage comparator is further adapted generate a control signal and transmit the control signal to the first core.

9. The semiconductor device of claim 8, wherein the control signal is an enable signal adapted to enable the data transfer between the first core and the second core.

10. The semiconductor device of claim 8, wherein the control signal is a disable signal adapted to disable the data transfer between the first core and the second core.

11. A method for controlling data transfer, comprising:

providing a transmitter, a receiver, and a transmission line for controlling the data transfer between a first core and a second core within a semiconductor device;

sending, by the transmitter, a signal over the transmission line to the receiver;

creating, by the receiver, an impedance mismatch to indicate that the second core is unable to transfer the data between the first core and the second core; and

detecting, by the transmitter, the impedance mismatch.

12. The method of claim 11, further comprising creating the impedance mismatch by changing an impedance of the transmission line.

13. The method of claim 11, further comprising using a capacitor in the receiver to change the impedance of the transmission line.

14. The method of claim 11, further comprising terminating by the transmitter, the data transfer upon detection of the impedance mismatch.

15. The method of claim 11, wherein the signal is a voltage signal; and

receiving by the transmitter, a reflection of the voltage signal.

16. The method of claim 15, wherein the transmitter comprises a voltage comparator; and

comparing by the voltage comparator, an amplitude of the voltage signal to an amplitude of the reflection of the voltage signal.

17. The method of claim 16, further comprising:

generating by the voltage comparator, a control signal; and

transmitting by the voltage comparator the control signal to the first core.

18. The method of claim 17, wherein the control signal is a disable signal, and further comprising

disabling by the disable signal, the data transfer between the first core and the second core.

19. The method of claim 11, further comprising:

creating by the receiver, an impedance match to indicate that the second core is able to transfer the data between the first core and the second core; and

detecting by the transmitter, the impedance match.

20. The method of claim 11, wherein the first core and the second core are selected from the group consisting of a microcontroller, a microprocessor, and an integrated circuit.